REMARKS

Claims 1-25 remain pending in the application. Claim 1-8 and 25 were previously withdrawn from consideration.

Claims 9-25 stand objected to because of certain informalities.

In response, Applicants have now amended claim 9 to incorporate the language suggested by the Examiner. Likewise, the identifier corresponding to claim 25 has been changed from "currently amend" to "withdrawn".

By making the above corrections, Applicants believe that they have not introduced new issues that may prompt the need for a new search. Applicants believe that the corrections have been incorporated to place the claims in better condition for Appeal.

Claims 9-11, 13-16, 18, 21 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (U.S. Pat 5,721,495) in view of Sugasawara (U.S. Pat. 6,043,672) and Teene (US. Pat 5,726,997).

Regarding the rejection of Claim 9, and more particularly, in answer to the Examiners' "Response to Arguments" (item 1, page 2 of the present Office Action) Applicants respectfully traverse the Examiner's arguments described therein regarding the combination of Jennion, Sagasawara and Teene.

Jennion teaches how to take an accurate and high resolution IDDQ measurement. The amount of current provided by the power supply dictates the scale used for the current measurement, and so the resolution. Jennion solves this problem by teaching an interface circuit between the IC under test and the IC tester, which senses when the IC has reached a quiescent current state, and switches from the high power supply to the IC tester parametric measurement unit capable of precisely measuring IDDQ. Jennion teaches taking an IDDQ measurement on a power distribution grid.

Applicant submit that the term "bus" as used in the present applicants differs from the term "bus" used by Teene, and that this difference needs to be recognized.

The "quiescent voltage bus" phrase used by Applicants in the present invention is a quiescent power distribution grid within the IC, separate from the global voltage bus. In paragraph [0023], the terms "distribution grid" and "bus' are clearly shown to be synonymous. Paragraph [0023] defines the global and quiescent power systems, including the global and quiescent power distribution grids or buses. In contradistinction, Teene utilizes the terminology "bus" used in "power supply bus" and "internal power bus" as segments of a **single** power distribution grid. For example, in Teene claim 1, "at least a first internal power bus electrically connected to said first power supply bus". More specifically, in Teenes' figures, the "power supply bus" and "internal power bus" are shown as wiring on different metal levels in the IC. From the Examiner's reply, Applicants submit that one of the differences between the Applicants' and the Examiner's interpretations of Teene is attributed to the terminology "bus" representing different parameters. As stated earlier, Applicants refer to it as an entire power distribution grid, whereas Teenes' teaching is directed to a wire segment in a power distribution grid.

Furthermore, the Examiner states that even though Teenes' "power supply bus" and "internal power bus" are electrically connected, they are deemed to be separate elements because they perform different functions. In Teenes' first three paragraphs of the DETAILED DESCRIPTION section (roughly column 2 – column 3 thru line 6), the function of both the "power supply bus" and "internal power bus" is described as follows:

"Power is distributed to the internal power busses 14 by supply busses 16 which run perpendicular to the internal power busses 14 in the illustrated embodiment. Standard or gate array cells 18 for performing the particular functions for which the circuit 10 is designed are positioned between the current monitoring cells 12, and power is provided to these cells 18 by the internal power busses 14."

From this excerpt and the remainder of the reference, the "power supply bus" and

"internal power bus" perform the same function, i.e., providing power to the IC standard or gate array cells. Teene, Figs 1 and 2 teaches this as well. Teenes' current monitoring circuits are located near the power grid connection points between the supply and the internal power busses. These circuits take advantage of the voltage differential between upstream (supply bus) and downstream (internal bus) segments of the power distribution (Applicants refer to it as the "global voltage bus"). The current monitoring circuits shunt some current around the power grid connection point through current measurement circuitry, which in Fig 2 is compared to a standard, and stored in a scan flip-flop. The power supply busses and internal power busses are independent of the current monitoring circuitry. If, "*arguendo*" the current monitoring circuits were removed from the design, both power supply busses and internal power busses still continue to be required because **they perform the same function,** i.e., to provide power to the IC cells. Applicants submit that these arguments refute the Examiner's argument that they have different functions.

The Examiner states that the method recited in claim 9 is allegedly obvious based on Jennion n view of Sagasawara and Teene. This rejection is traversed for several reasons

1) Jennion does not teach nor suggest constructing a power distribution or circuit connection to power/ground within an IC powering the chip by way of a global voltage bus setting it in a quiescent state.
2) Jennion teaches switching to appropriate current supply/ measurement electronics to make a high resolution current measurement. Circuit selection and routing using a quiescent power bus is not an obvious extension of using a multiplexer to select a power input.
3) Regarding the combination of Jennion and Teene, Teene is a direct extension of Jennion. As described above, the IC power distribution grid is essentially unchanged between Jennion and Teene. Teene moves the current measurement circuitry on-chip. If Teene were implemented on an IC, there would be no reason to add a quiescent power distribution grid to the IC design. Thus, Teene teaches away from Applicants' teaching.

Regarding the combination of Teene and Jennion to Sagasawara, Applicants submit that:

4) Adding Sagasawara to the combination of Teene and Jennion has Jennion teaching performing a tester based IDDQ current measurement on an IC power grid, Teene detecting current associated with defects by adding local current monitors to the IC power grid and Sagasawara adding routing circuitry to the power grid to disconnect sections from the main power input and connect them to a second power input, which teaches away from the Applicants who teach a global power grid, a quiescent power grid, and header switches that can be used to select which functional circuits load the power grids.

5) Moreover, Teene, Jennion, and Sagasawara in combination are not even compatible implementations. It would be difficult to implement any of the stated teachings on the same IC circuitry. All three on-chip implementations address improving IDDQ measurement by using on-chip circuitry to reduce the amount of IC circuitry that is being measured or monitored. However i**f Teene were combined to Jennion, the resultant combination Teene-Jennion is not only redundant but Teene compromises Jennions' measurements.**

6) Furthermore, Jennion describes tester based IDDQ test. Teene moves IDDQ test on-chip to avoid the need for Jennion IDDQ test. When Teene is actively monitoring current on-chip, current measurements using Jennion will include the current drawn by current monitoring circuits and by standard and/or gate array cells. Once again, Teenes' current monitors compromise Jennions' IDDQ measurement.

7) In cases when an IC displays a "good" IDDQ, using Jennion's teaching will adjust to a sufficiently high resolution measurement and detect the defective current. In

such cases, Jennion's method will not be effective for identifying the defective ICs altogether.

8) Now, adding Sagasawara to the combination of Teen and Jennion does not resolve any of the problems introduced by merging the teachings of Teene and Jennion.

Accordingly, Applicants believe that Claim 9 is free of rejection under 35 U.S.C. 103(a) as being allegedly unpatentable over Jennion in view of Sugasawara and Teene, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Regarding the rejection of claims of claims 10-20, Applicants submit that since the combination of Jennion, Sugasawara and Teene does not render claim 9 to be unpatentable, neither is the combination of the three references renders claims 10-21, that depend on claim 9.

Applicants believe that Claims 9, 10-20 is free of rejection under 35 U.S.C. 103(a) as being unpatentable over Jennion in view of Sugasawara and Teene, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 21-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Jennion et al. (US Pat 5,721,495) in view of Sugasawara (US Pat. 6,043,672) and Teene (US. Pat 5,726,997) and further in view of Akiki et al. (U.S Pat. 5,294,883)

Applicants submit that since the combination of Jennion, Sugasawara and Teene does not render claim 21 to be unpatentable for the reasons advanced previously, by adding Akiki to the combination of Jennion, Teene and Sagasawara does not render unpatentable claim 21 and/or claims 22-24 which are dependent thereof.

The previous stated argument also applies to the rejection of claim 17, based on the combination of Jennion, Sugasawara and Teene in view of Cole Jr. (U.S. Pat. 6,031,386)

Therefore, Applicants respectfully submit that claims 21-24 are patentable both over Jennion, Sugasawara and Teene in view of Akiki, and over Jennion, Sugasawara and Teene in view of Cole.

Thus, Applicants respectfully request that claims 10-20 and 21-24 are free of rejection under 35 U.S.C § 103(a) in view, respectively of Jennion in view of Sugasawara ,Teene and Akiki, and of Jennion in view of Sugasawara ,Teene and Cole, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing, it is respectfully requested that all the outstanding objections and rejections to this application be reconsidered and withdrawn, and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,

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